HIGH-VOLTAGE DIGITAL-SIGNAL IC

UCi7701

160-Output LCD SEG/COM Driver

MP Specifications **April 2, 2012**

ULTRACHIP

The Coolest LCD Driver, Ever!

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UCi7701

160-Output LCD SEG/COM Driver

INTRODUCTION

UCi7701c is a 160-bit output SEG/COM driver LSI, suitable for driving the large scale dot matrix LCD panels used by PDA's, personal computers and work stations for example. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module.

UCi7701c is good as both a SEG driver and a COM driver. A low power consuming, high-precision LCD panel display can be assembled using the UCi7701c. In SEG mode, the data input is selected 4-bit parallel input mode or as 8-bit parallel input mode by a mode pin (MD). In COM mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

FEATURE HIGHLIGHTS

(SEG mode)

- Shift Clock frequency :
  - 14 MHz (Max.) (V_{DD} = 5V ± 10%)
  - 8 MHz (Max.) (V_{DD} = 2.5V - 4.5V)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode pin (MD)
- Automatic transfer function with an enable signal
- Automatic counting function when in the chip select mode, causes the internal clock to be stopped by automatically counting 160 bits of input data

(COM mode)

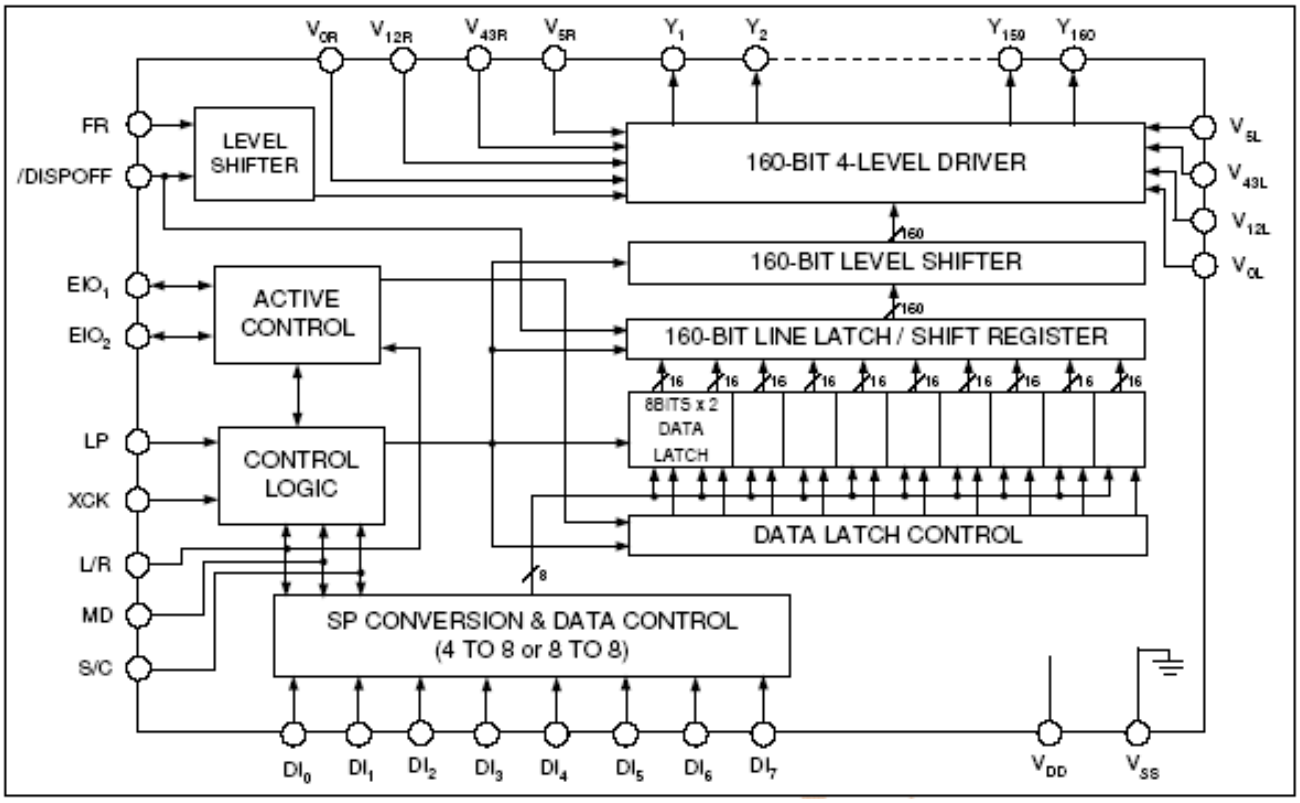
- Shift clock frequency: 4.0MHz (Max.)
- Built-in 160-bit bi-directional shift register (divisible into 80-bit x 2)
- 4 pin-selectable shift directions available in single mode (160-bits shift register) or dual mode (80-bits shift register x 2)

  1. Y1 → Y160 (Single mode)
  2. Y160 → Y1 (Single mode)
  3. Y1 → Y80, Y81 → Y160 (Dual mode)
  4. Y160 → Y81, Y80 → Y1 (Dual mode)

(Both SEG mode and COM mode)

- Supply voltage for LCD drive: 15.0 to 42V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5V
- COMs process
- Package: 190-pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UCi7701cGAC-U0P	Bump on Chip Tray
UCi7701cTAC-U0	TCP Form

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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CAUTIONS CONCERNING STORAGE

1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions :

Storage state	Storage conditions
Unopened (less than 90 days)	Temperature: 5 to 30℃; humidity: 80%RH or less
After seal of broken (less than 30 days)	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

CONTACT DETAILS

UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

PIN DESCRIPTION

<table>
<tr><th>Pin Name (Pad Name)</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td>VDD</td><td>PWR</td><td>3</td><td>Power supply pin for the logic system (+2.5 to +5.5V)</td></tr>
<tr><td>Vss</td><td>GND</td><td>11</td><td>Ground (0V).</td></tr>
<tr><td>V0R, V0L (V0)
V12R, V12L (V12)
V43R, V43L (V34)
V5R, V5L (V5)</td><td>PWR</td><td>1, 1
1, 1
1, 1
1, 1</td><td>Bias power supply pin for LCD driver voltage.
Normally, the bias voltages are set by a resistor divider.
Ensure that voltages are set such that Vss ≤ V5 < V34 < V12 < V0.
To reduce the differences between the output waveforms of the LCD driver output pins Y1 and Y160, connect externally V0R and V0L, V12R and V12L, V43R and V43L, respectively.</td></tr>
<tr><td>D7 ~ D0 (DI7~DI0)</td><td>I</td><td>8</td><td>For COM mode
Data input for Dual mode. According to the data shift direction of the data shift register, data can be input starting from the 81st bit.
<table>
<tr><th></th><th>D7</th><th>D6~D0</th></tr>
<tr><td>Single mode</td><td>won't be pulled down</td><td rowspan="2">Not used. Connect to VDD or Vss to avoid floating.</td></tr>
<tr><td>Dual mode</td><td>will be pulled down</td></tr>
</table>
For SEG mode
Input for Display data
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>4-bit mode</td><td colspan="4">Connect to VDD or Vss</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td></tr>
<tr><td>8-bit mode</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td></tr>
</table></td></tr>
<tr><td>XCK</td><td>I</td><td>1</td><td>For COM mode
Not used. Pull down and connect to Vss or leave it open.
For SEG mode
Clock input for display data. Data are read on the falling edge of clock pulse.</td></tr>
<tr><td>LP</td><td>I</td><td>1</td><td>For COM mode
Shift clock input for bi-directional shift register. Data are shifted at the falling edge of clock pulse.
For SEG mode
Latch pulse input for display data. Data are latched on the falling edge of clock pulse.</td></tr>
<tr><td>L/R</td><td>I</td><td>1</td><td>Shift direction (Left / Right) selection for reading display data.
When L/R is set to “L” (Vss level), data are read sequentially from Y160 to Y1.
When L/R is set to “H” (VDD level), data are read sequentially from Y1 to Y160.</td></tr>
<tr><td>$\overline{\text{DISPOFF}}$
(/DISPOFF)</td><td>I</td><td>1</td><td>Control for output of non-select level. The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.
When set to “L”, the LCD drive output pins (Y1~Y160) are set to level V5 and the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of $\overline{\text{DISPOFF}}$. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs non-select level (V12 or V34), then outputs the contents of the data latch on the next falling edge of the LP. At that time, if $\overline{\text{DISPOFF}}$ removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly.</td></tr>
<tr><td>FR</td><td>I</td><td>1</td><td>AC-converting signal input for LCD driver waveform. The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage level can be set using the line latch output signal and the FR signal.</td></tr>
</table>

<table>
<tr><th>Pin Name (Pad Name)</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td>MD</td><td>I</td><td>1</td><td>Single or Dual (or 4-bit or 8-bit) Mode selection.
For COM mode
When MD is set to “L”, Single mode is selected.
When MD is set to “H”, Dual mode is selected.

For SEG mode
When MD is set to “L”, 4-bit parallel input mode is selected.
When MD is set to “H”, 8-bit parallel input mode is selected.</td></tr>
<tr><td>S/C</td><td>I</td><td>1</td><td>SEG mode / COM mode selection.
When S/C is set to “L”, COM mode is selected.
When S/C is set to “H”, SEG mode is selected.</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>1, 1</td><td>For COM mode
Data input / output for the bi-directional shift register.
<table>
<tr><td></td><td>EIO2</td><td>EIO1</td></tr>
<tr><td>L/R=”L”</td><td>used as input. pulled down.</td><td>used as output</td></tr>
<tr><td>L/R=”H”</td><td>used as output</td><td>used as input. pulled down</td></tr>
</table>
For SEG mode
Input / output for chip select.
<table>
<tr><td></td><td>EIO2</td><td>EIO1</td></tr>
<tr><td>L/R=”L”</td><td>used as input</td><td>used as output</td></tr>
<tr><td>L/R=”H”</td><td>used as output</td><td>used as input</td></tr>
</table>
During output, it’s set to "H" while LP • XCK is "H" and after 160 bits of data have been read, it’s set to "L" for one cycle (from one falling edge to its next falling edge of XCK), after which it returns to "H".
During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is deselected after 160 bits of data have been read.</td></tr>
<tr><td>Y160 ~ Y1</td><td>O</td><td>160</td><td>LCD driver output.
Corresponding directly to each bit of the data latch, one level (V0, V12, V34, or V5) is selected and output.</td></tr>
<tr><td>Dummy</td><td></td><td>18</td><td>No connection.</td></tr>
</table>

S/C	MD	L/R	EIO2	EIO1
L: COM mode	L: SINGLE mode	L: Data shifted Y160 → Y1	Input	Output
		H: Data shifted Y1 → Y160	Output	Input
	H: DUAL mode	L: (same)	(same)	(same)
		H: (same)	(same)	(same)
H: SEG mode	L: 4-bit mode	L: Data shifted Y160 → Y1	Input	Output
		H: Data shifted Y1 → Y160	Output	Input
	H: 8-bit mode	L: (same)	(same)	(same)
		H: (same)	(same)	(same)

FUNCTIONAL OPERATIONS

1. Block description

1.1. Active Control
In the case of segment mode, controls the selection or deselection of the chip. Following a LP signal input, and after the select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the ship is deselected.

In the case of common mode, controls the input/output data of bidirectional pins.

1.2. SP Conversion & Data Control
In the case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

1.3. Data Latch Control
In the case of the segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

1.4. Data Latch
In the case of the segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control 160 bits of data are read in 20 sets of 8 bits.

1.5. Line Latch / Shift Register
In the case of the segment mode, all 160 bits which have been read into the data latch, are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block.

In the case of the common mode, shifts data from the data input pin on to the falling edge of the LP signal.

1.6. Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

1.7. 4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V0, V12, V43, Vss) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

1.8. Control Logic
It controls the operation of each block. In the case of the segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

In the case of the common mode, it controls the direction of the data shift.

2. LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

2.1. Segment Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y1 ~ Y160)
L	L	H	V43
L	H	H	V5
H	L	H	V12
H	H	H	V0
X	X	L	V5

Remark:
VSS <= V5 < V43 < V12 <V0,
H: VDD (+2.5 to +5.5V),
L: VSS (0V),
X: Don't care

2.2. Common Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y1 ~ Y160)
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	V5
X	X	L	V5

Remark:
VSS <= V5 < V43 < V12 < V0,
H: VDD (+2.5 to +5.5V),
L: Vss (0V),
X: Don't care

Note:
1. There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which assigned by specification for each power pin.
2. That time "Don't care" should be fixed to "H" or "L", to avoid floating.

3. Relationship between the Display Data and Driver Output Pins

3.1. SEG Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					40clock	39clock	38clcok	…	3clock	2clock	1clock
L	L	Output	Input	D0	Y1	Y5	Y9	…	Y149	Y153	Y157
				D1	Y2	Y6	Y10	…	Y150	Y154	Y158
				D2	Y3	Y7	Y11	…	Y151	Y155	Y159
				D3	Y4	Y8	Y12	…	Y152	Y156	Y160
L	H	Input	Output	D0	Y160	Y156	Y152	…	Y12	Y8	Y4
				D1	Y159	Y155	Y151	…	Y11	Y7	Y3
				D2	Y158	Y154	Y150	…	Y10	Y6	Y2
				D3	Y157	Y153	Y149	…	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					20clock	19clock	18clcok	…	3clock	2clock	1clock
H	L	Output	Input	D0	Y1	Y9	Y17	…	Y137	Y145	Y153
				D1	Y2	Y10	Y18	…	Y138	Y146	Y154
				D2	Y3	Y11	Y19	…	Y139	Y147	Y155
				D3	Y4	Y12	Y20	…	Y140	Y148	Y156
				D4	Y5	Y13	Y21	…	Y141	Y149	Y157
				D5	Y6	Y14	Y22	…	Y142	Y150	Y158
				D6	Y7	Y15	Y23	…	Y143	Y151	Y159
				D7	Y8	Y16	Y24	…	Y144	Y152	Y160
H	H	Input	Output	D0	Y160	Y152	Y144	…	Y24	Y16	Y8
				D1	Y159	Y151	Y143	…	Y23	Y15	Y7
				D2	Y158	Y150	Y142	…	Y22	Y14	Y6
				D3	Y157	Y149	Y141	…	Y21	Y13	Y5
				D4	Y156	Y148	Y140	…	Y20	Y12	Y4
				D5	Y155	Y147	Y139	…	Y19	Y11	Y3
				D6	Y154	Y146	Y138	…	Y18	Y10	Y2
				D7	Y153	Y145	Y137	…	Y17	Y9	Y1

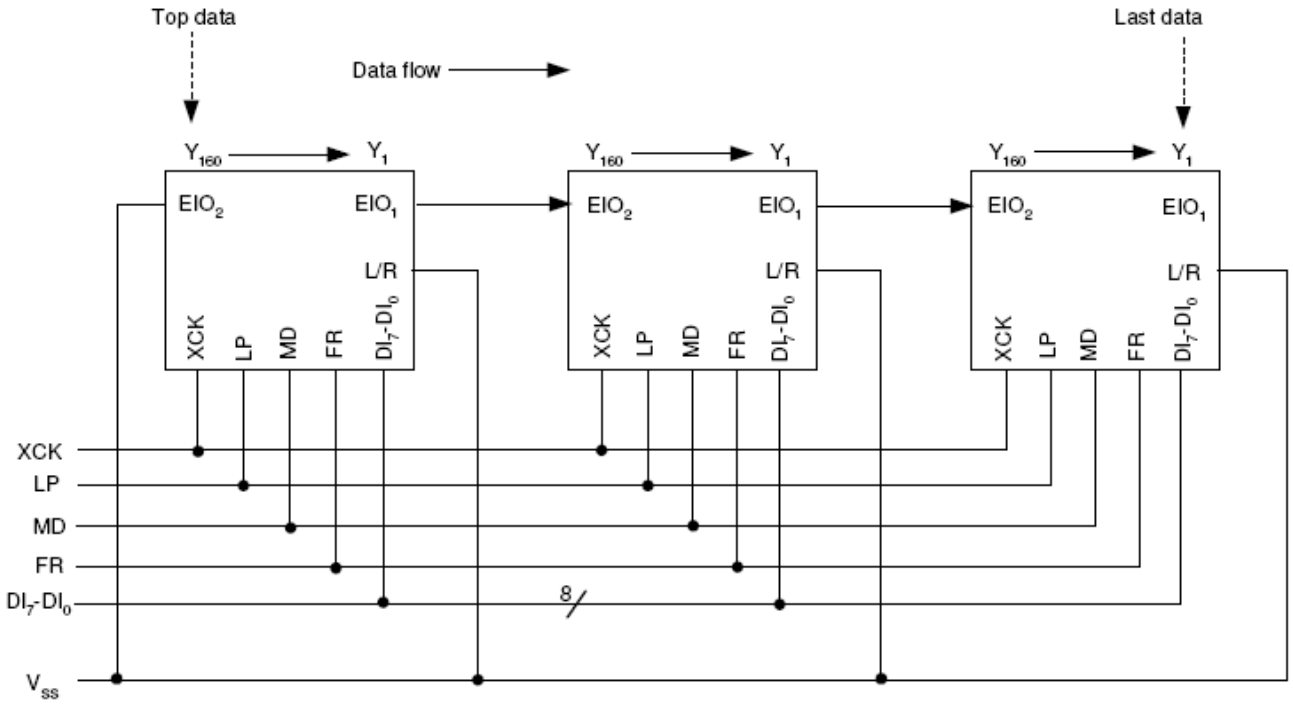
3.2. COM Mode

MD	L/R	Data Transfer Direction	EIO1	EIO2	D7
L (Single)	L (shift to left)	Y160 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y160	Input	Output	X
H (Dual)	L (shift to left)	Y160 to Y81, Y80 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y80, Y81 to Y160	Input	Output	Input

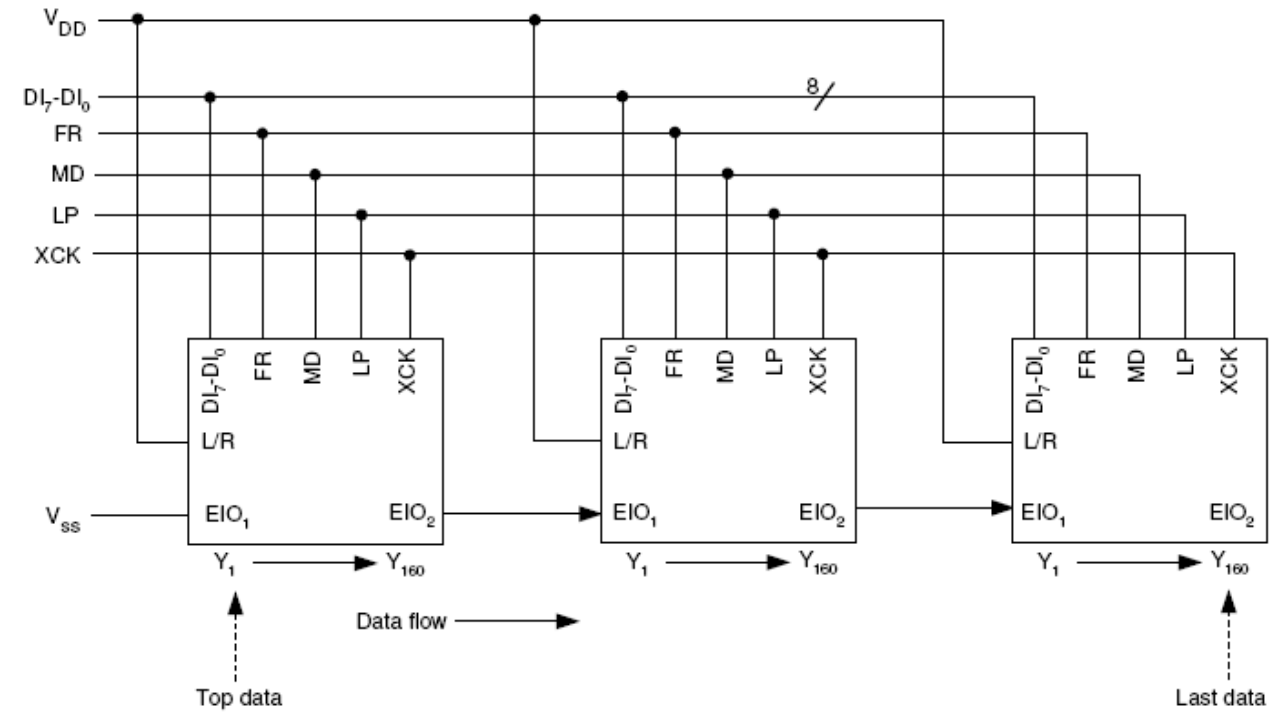
Remark:
L: Vss (0V),
H: V_{DD} (+2.5V to +5.5V),
X: Don't care. Should be fixed to "H" or "L", to avoid floating.

4. Connection Examples of SEG Drivers

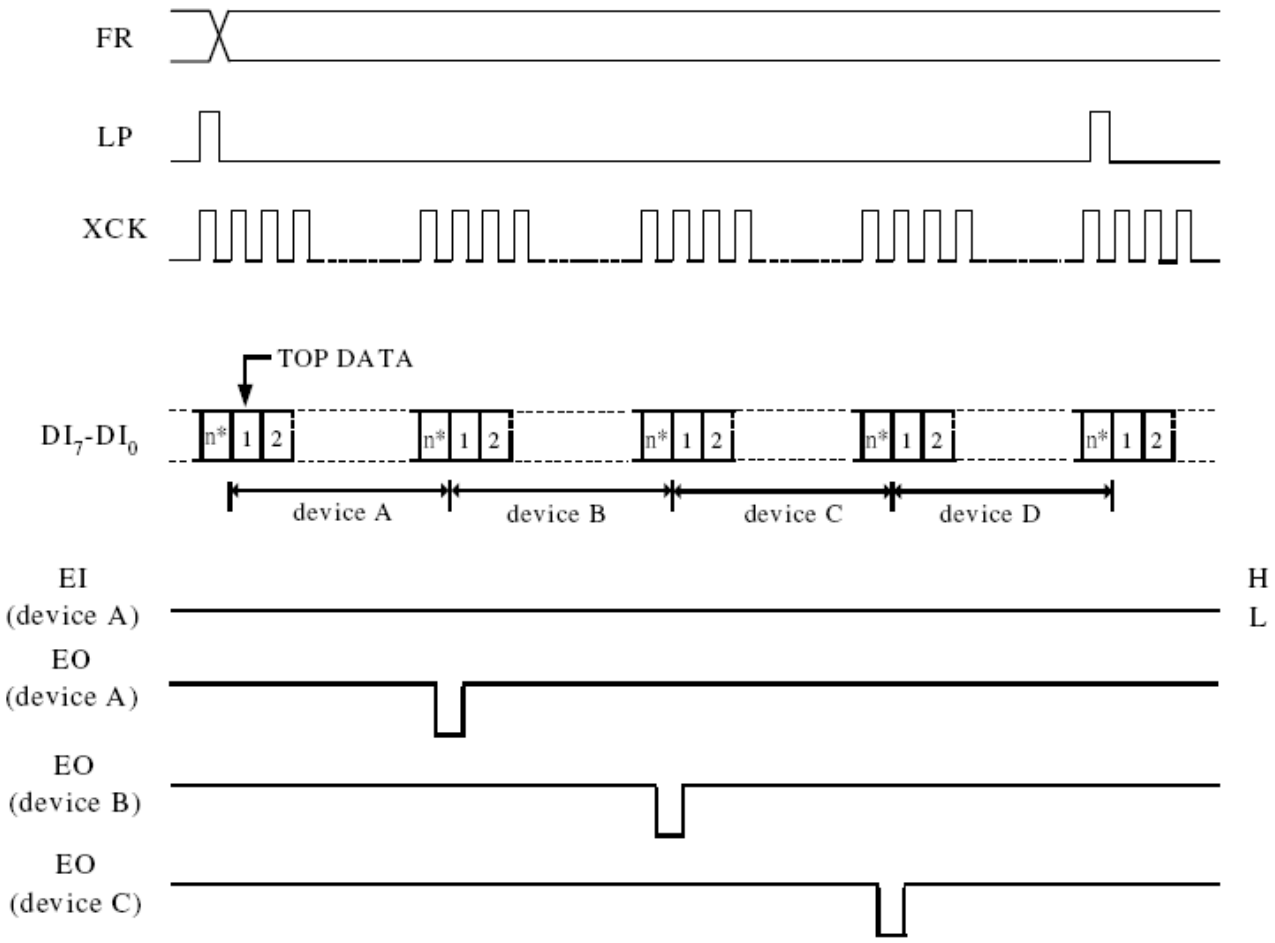
4.1. Case of L/R = "L"



4.2. Case of L/R = "H"



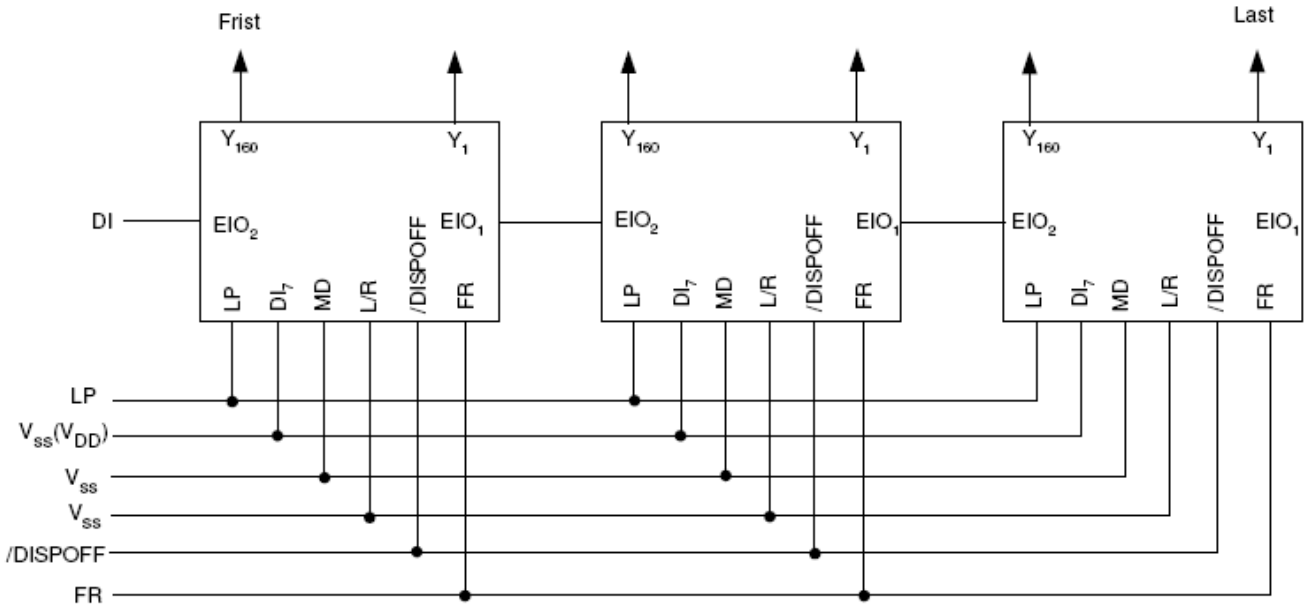
5. Timing Waveform of 4-Device Cascade Connection of SEG Drivers



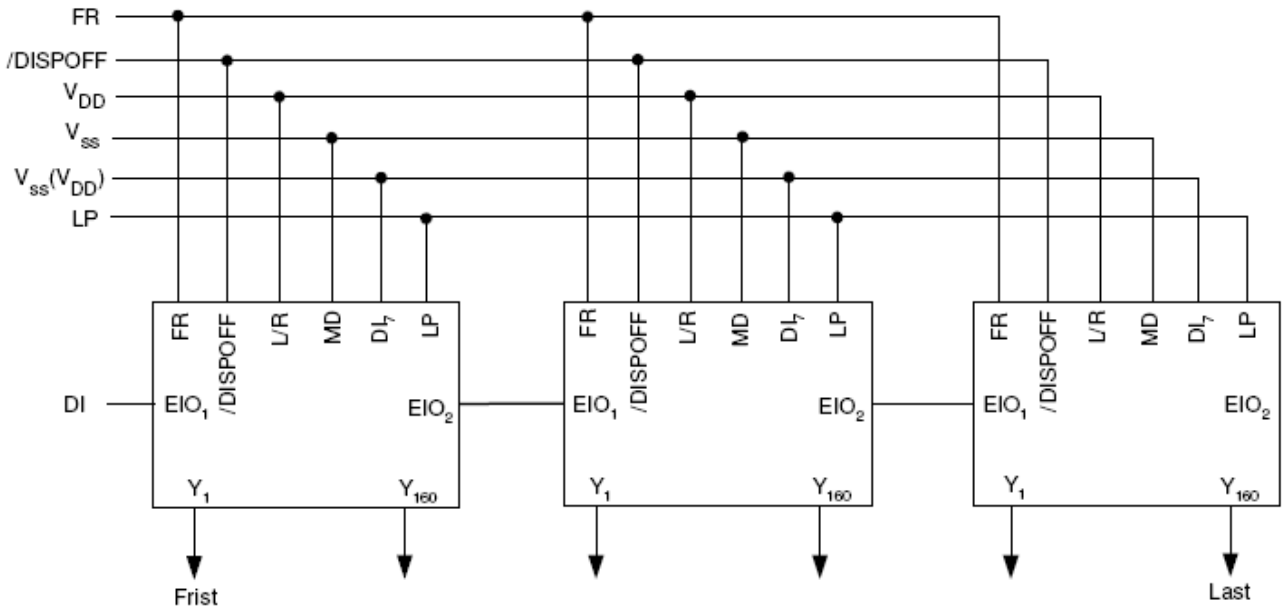
* n=40 in 4-bit parallel input mode
n=20 in 8-bit parallel input mode

6. Connection Examples for COM Drivers

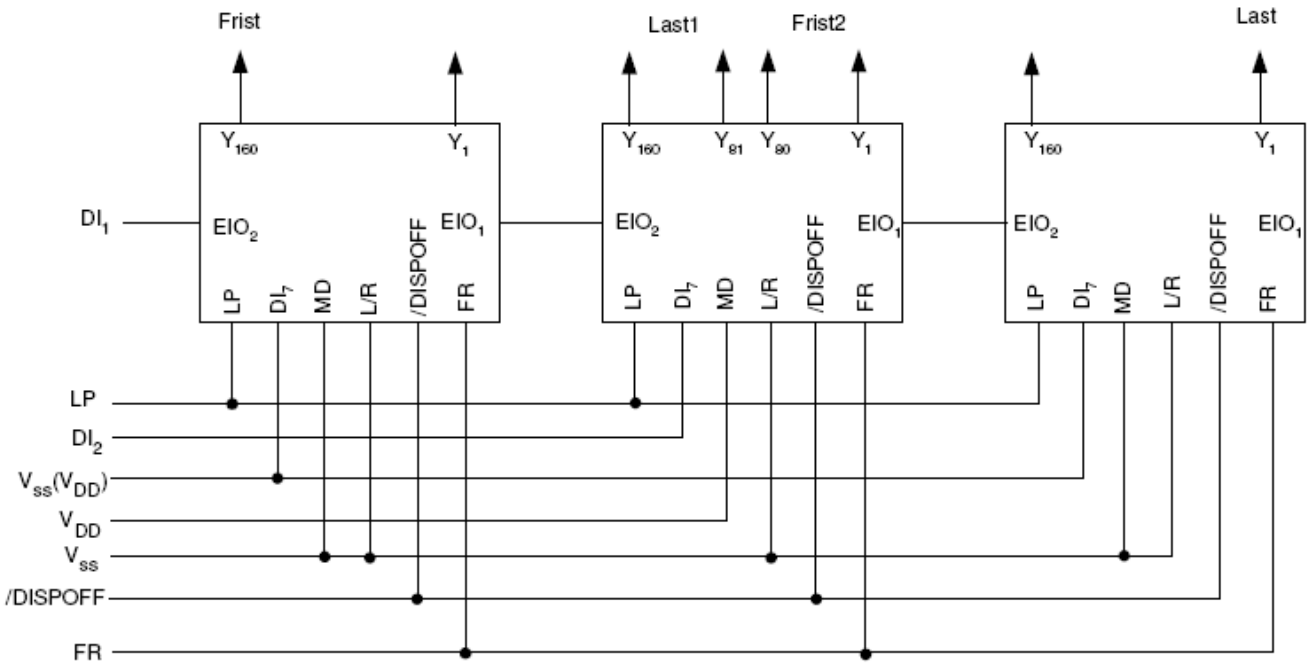
6.1. Single Mode (MD="L") **with L/R = "L"** (Data shifted Y160 → Y1, EIO2: input, EIO1: output)



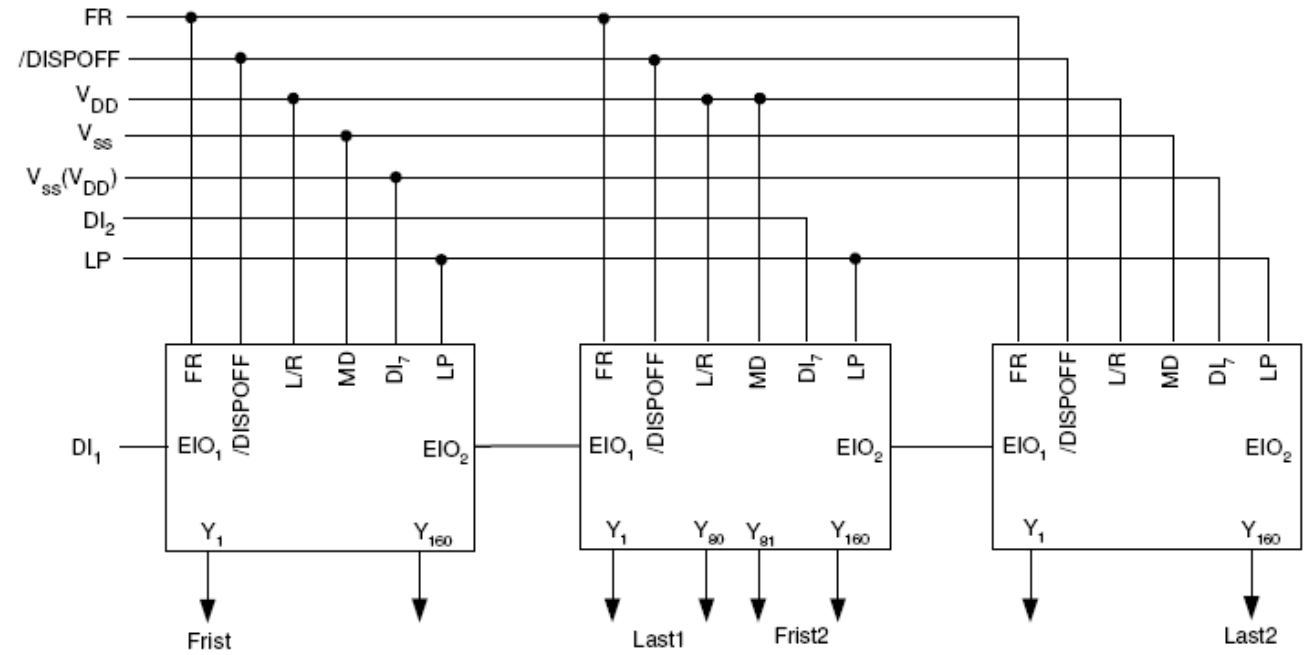
6.2. Single Mode (MD="L") **with L/R = "H"** (Data shifted Y1 → Y160, EIO2: output, EIO1: input)



6.3. Dual Mode (MD="H") **with L/R = "L"** (Data shifted Y160 → Y1, EIO2: input, EIO1: output)



6.4. Dual Mode (MD="H") **with L/R = "H"** (Data shifted Y1 → Y160, EIO2: output, EIO1: input)



7. Precaution

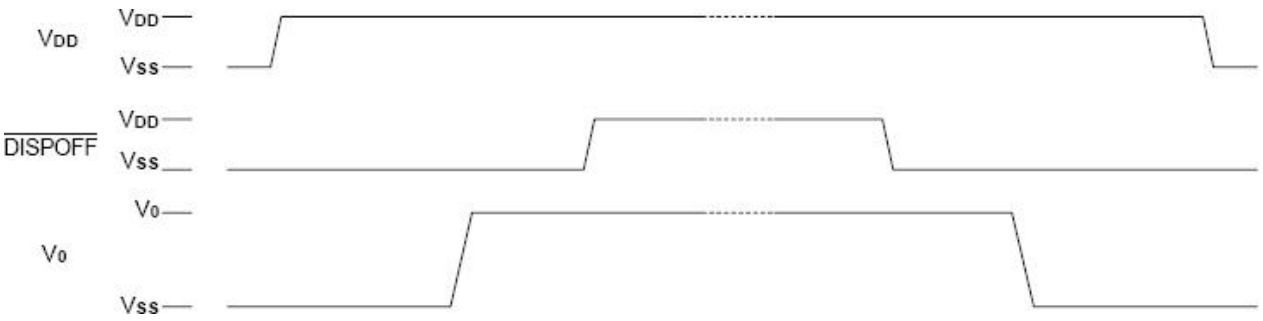
Be careful when connecting or disconnecting the power. This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

The details are as follows:

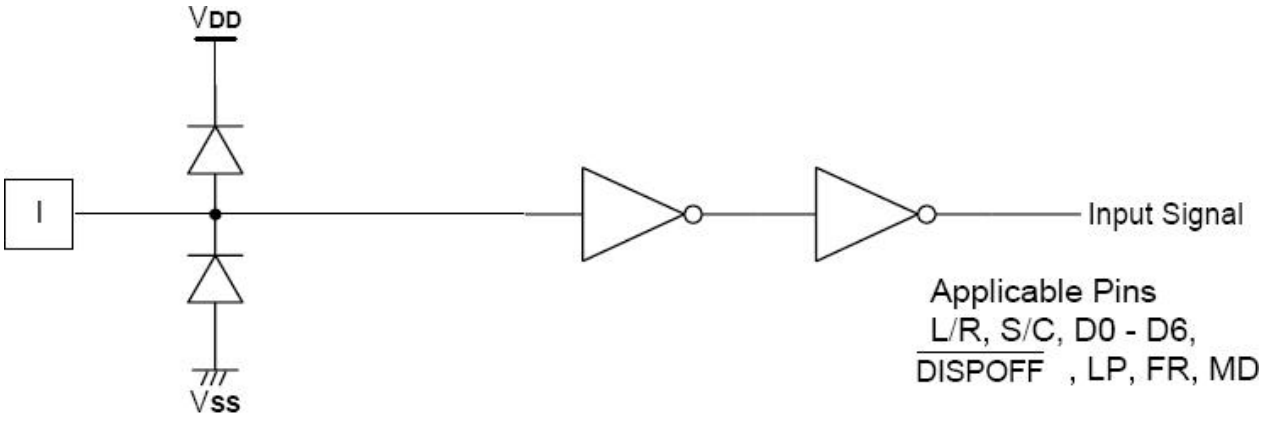
- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100Ω) or fuse to the LCD driver power V0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level VSS on the DISPOFF function. After that, disconnect the logic system power after disconnecting the LCD driver power.

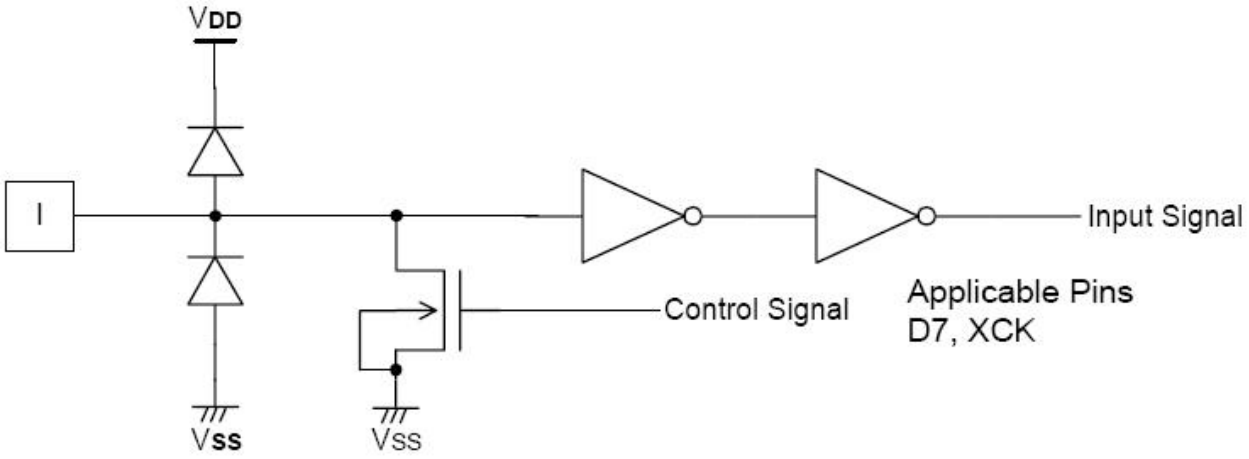
When connecting the power supply, follow the recommended sequence shown.



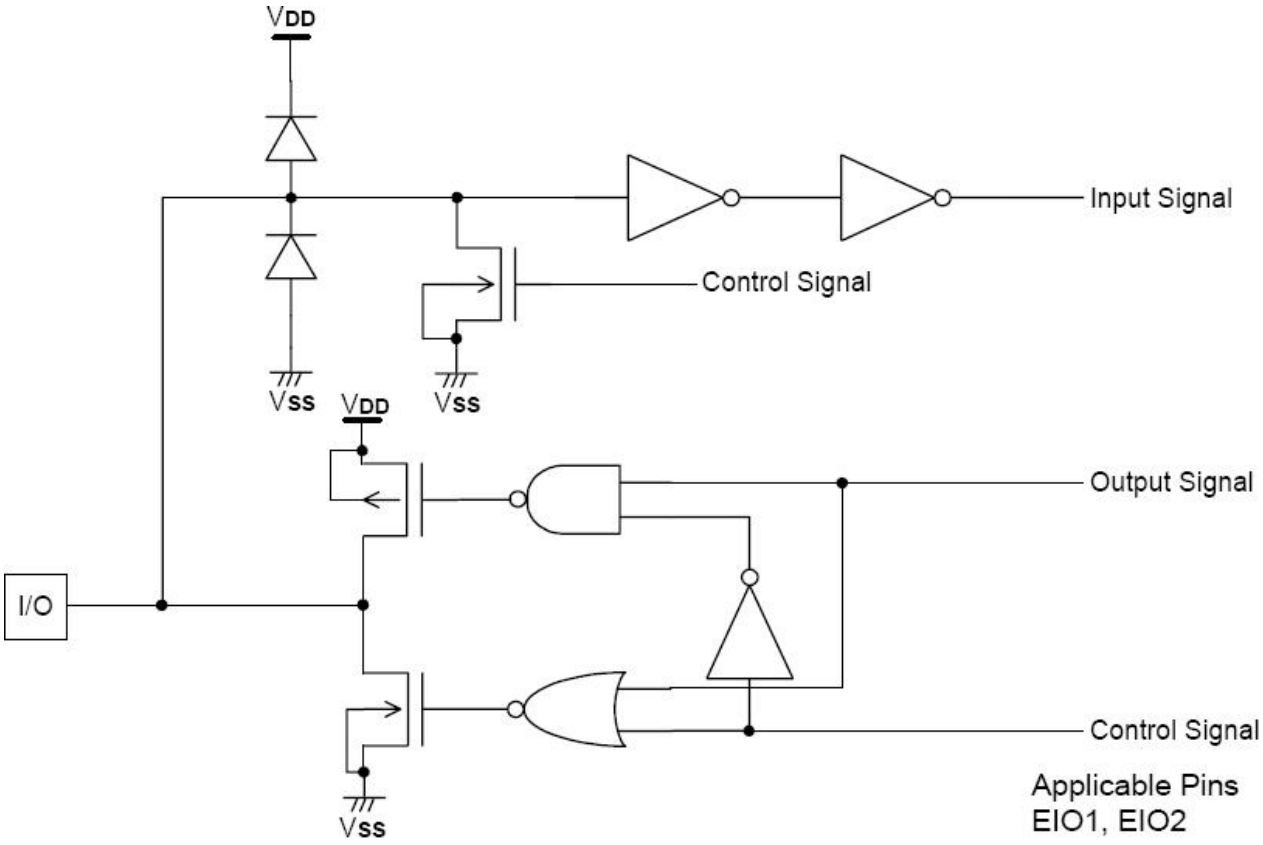
INPUT / OUTPUT CIRCUITS



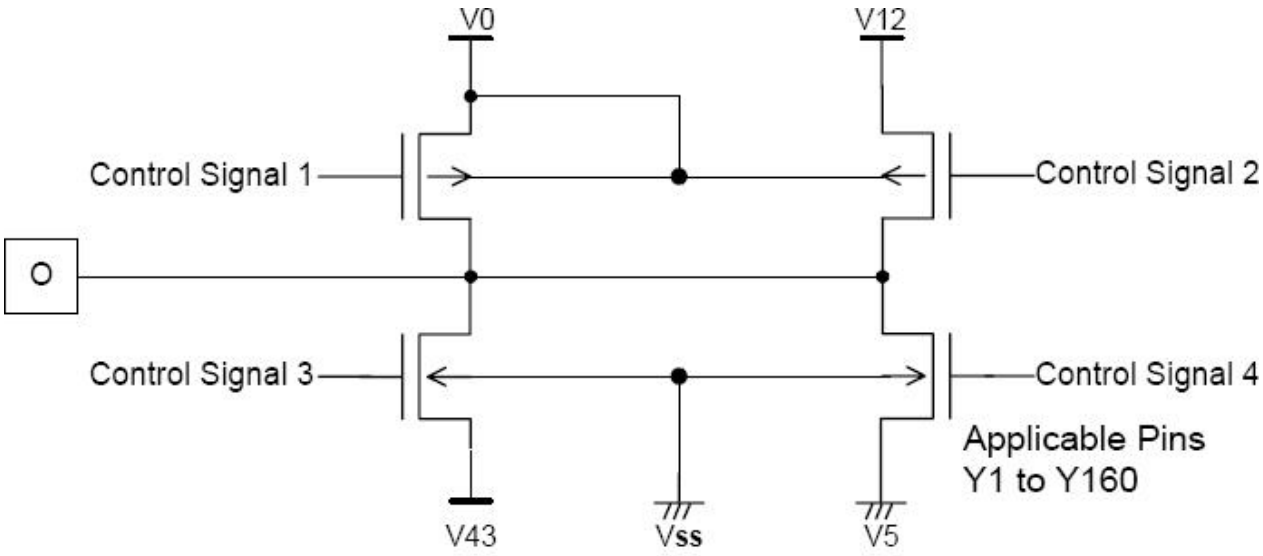
Input Circuit (1)



Input Circuit (2)

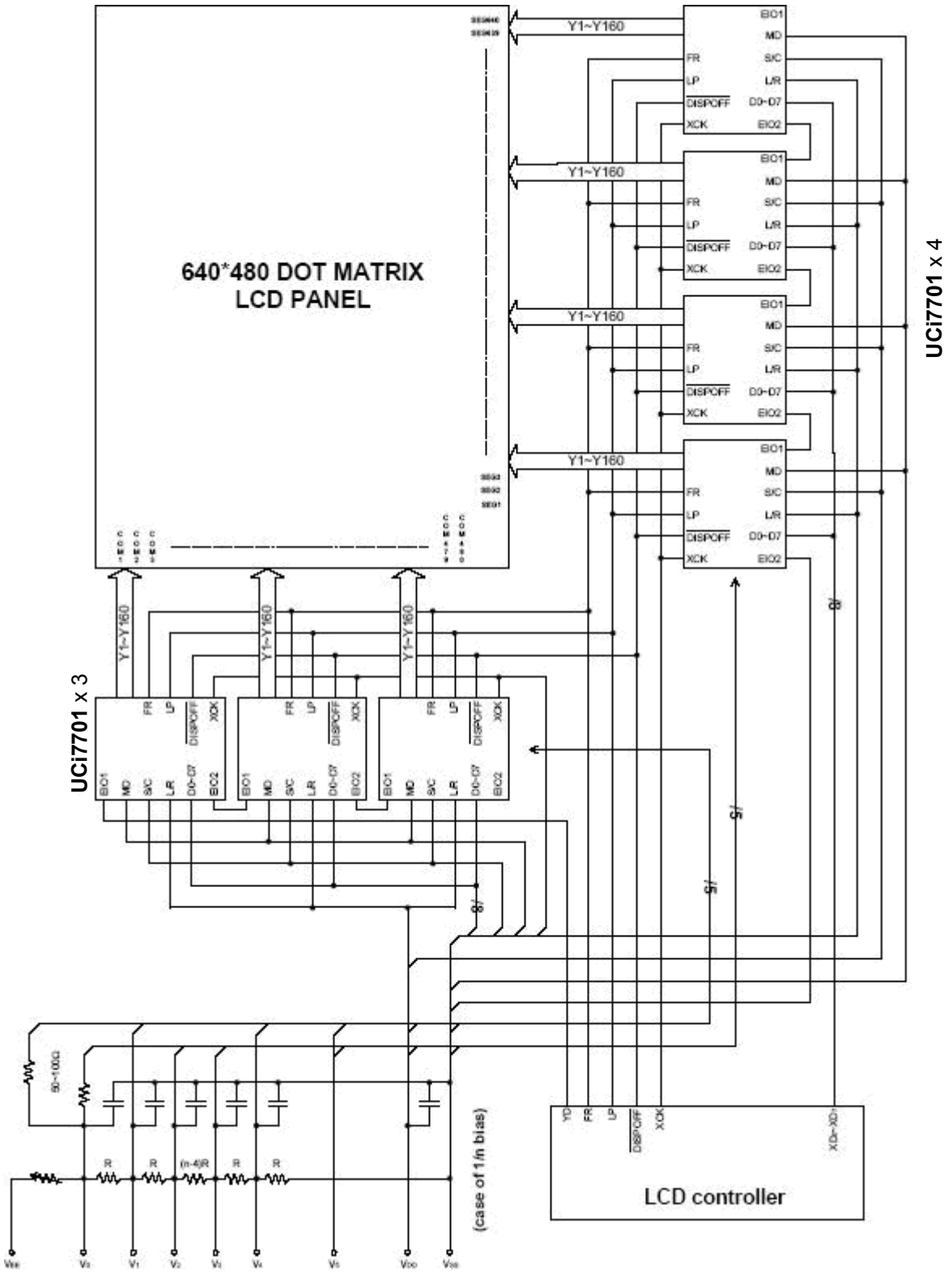


Input / Output Circuit

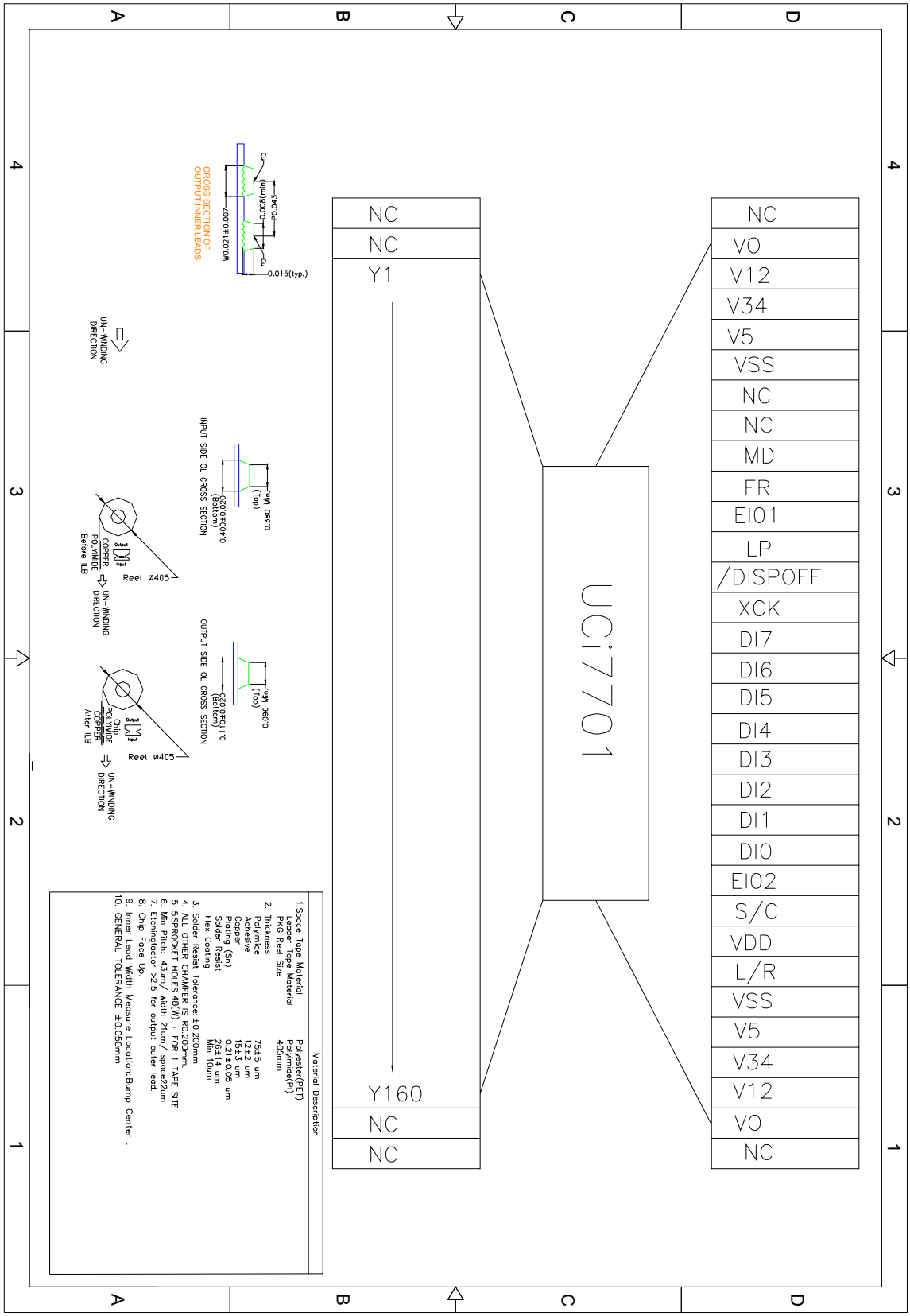


LCD Driver Output circuit

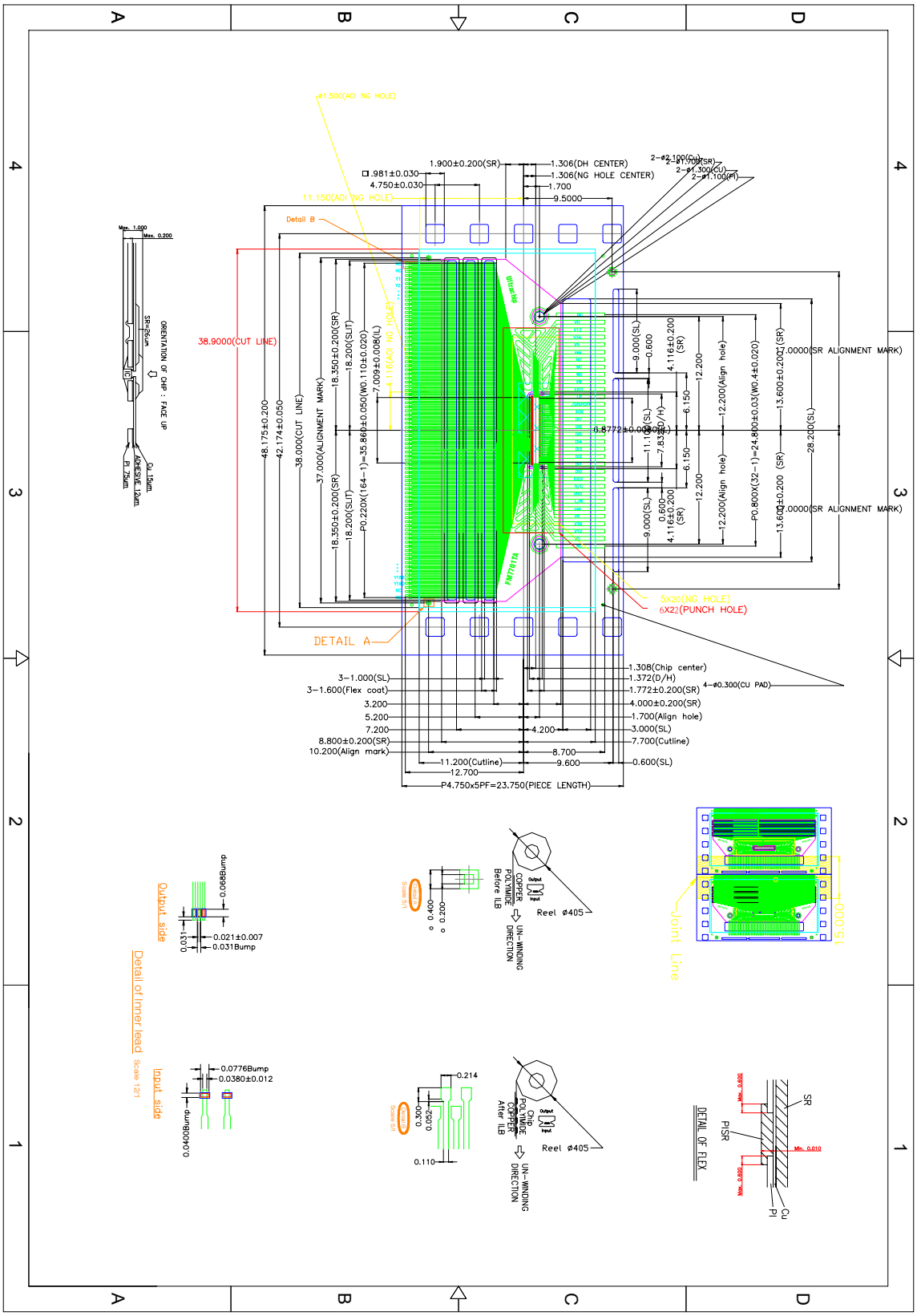
REFERENCE APPLICATION CIRCUIT



TCP PIN LAYOUT



EXTERNAL VIEW OF TCP PINS



ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Signal	Item	Rating
V_{DD}	DC Supply Voltage	–0.3V ~ +7.0V
V_0	DC Supply Voltage	–0.3V ~ +45V
V_{IN}	Input Voltage	–0.3V ~ V_{DD}+0.3V
T_{OPR}	Operating Ambient temperature	–30°C ~ +85°C
T_{STG}	Storage temperature	–45°C ~ +125°C

Remark: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

SEG Mode

(VSS = V5 = 0V, V_{DD} = 2.5 - 5.5V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.5	-	5.5	V	
Operating Voltage	V0	15	-	42	V	
Input high voltage	VIH	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins
Input low voltage	VIL	-	-	0.2 V_{DD}	V	
Output high voltage	VOH	V_{DD} - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA
Output low voltage	VOL	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA
Input leakage current 1	IIH	-	-	+1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, VI = V_{DD}
Input leakage current 2	IIL	-	-	-1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, VI = VSS
Output resistance	RON	-	1.0	1.5	kΩ	V0 = +42V | Y1 - Y160 pins, | ΔVON| = 0.5V
		-	1.5	2.0		V0 = +20.0V
Stand-by current	ISB	-	-	5	μA	Vss pin, See Note 1
Consumed current (1) (Deselection)	IDD1	-	-	2.0	mA	V_{DD} pin, See Note 2
Consumed current (2) (Selection)	IDD2	-	-	8.0	mA	V_{DD} pin, See Note 3
Consumed current	I0	-	-	1.0	mA	V0 pin, See Note 4

Note:

1. V_{DD} = +5.0V, V0 = +42V, VI = VSS
2. V_{DD} = +5.0V, V0 = +42V, fXCK = 14MHz, No-load, EI = V_{DD}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
3. V_{DD} = +5.0V, V0 = +42V, fXCK = 14MHz, No-load. EI = VSS
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. V_{DD} = +5.0V, V0 = +42V, fXCK = 14MHz, fLP = 41.6kHz. fFR = 80 Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)

COM Mode

(Vss = V5 = 0V, V_{DD} = 2.5 - 5.5V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

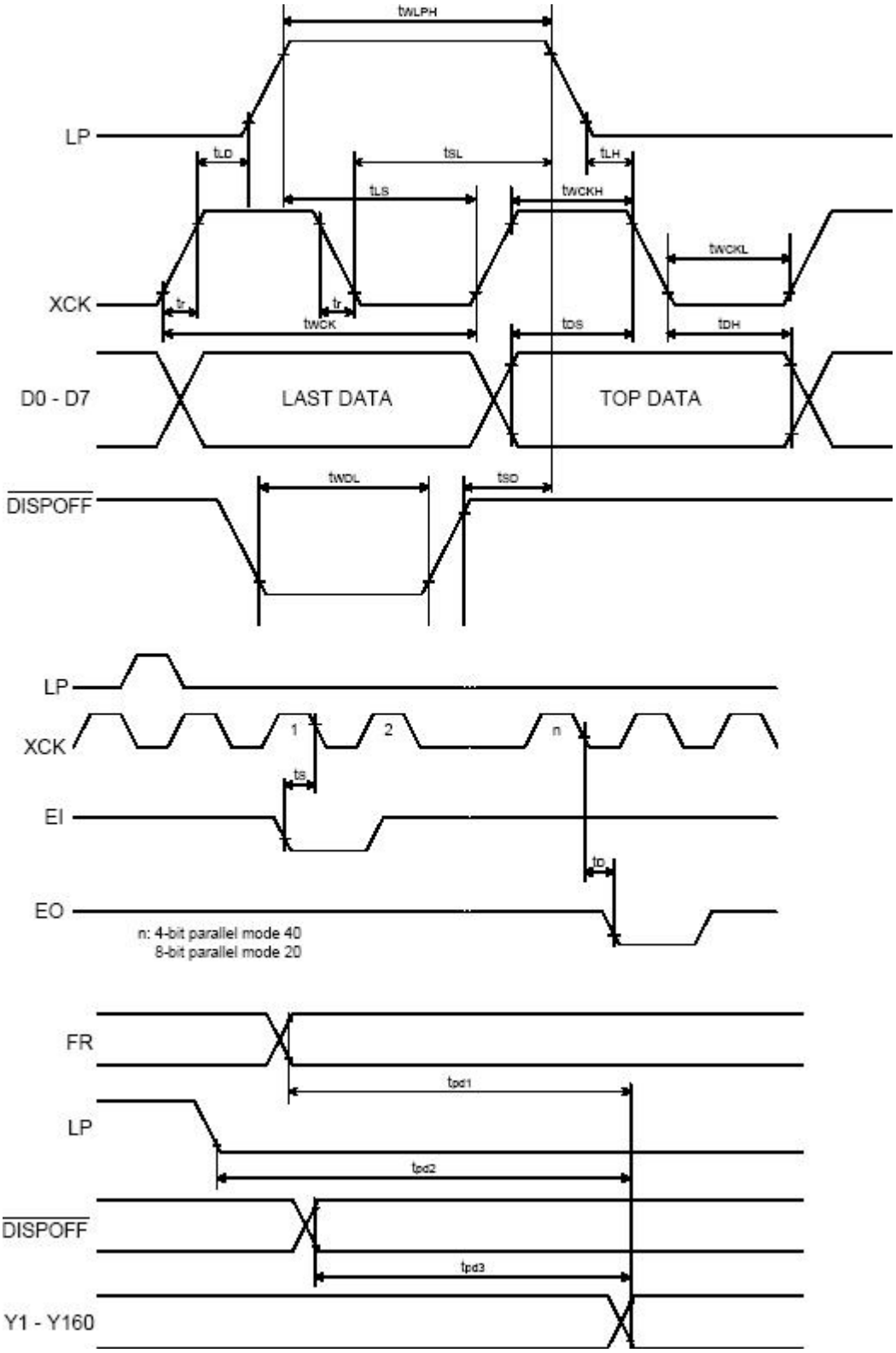
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.5	-	5.5	V	
Operating Voltage	V0	15	-	42	V	
Input high voltage	VIH	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins
Input low voltage	VIL	-	-	0.2 V_{DD}	V	
Output high voltage	VOH	V_{DD} - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA
Output low voltage	VOL	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA
Input leakage current 1	IIH	-	-	+10.0	μA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, VI = V_{DD}
Input leakage current 2	IIL	-	-	-10.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, VI = VSS
Output resistance	RON	-	1.0	1.5	kΩ	V0 = +42V | Y1 ~ Y160 pins, | ΔVON| = 0.5V
		-	1.5	2.0		V0 = +20.0V
Stand-by current	ISB	-	-	50	μA	VSS pin, Note 1
Consumed current (1)	IDD	-	-	80	μA	V_{DD} pin, Note 2
Consumed current (2)	I0	-	-	160	μA	V0 pin, Note 2

Note:

1. V_{DD} = +5.0V, V0 = +42V, fLP = 0 - 41.6kHz
2. V_{DD} = +5.0V, V0 = +42V, fLP = 41.6KHz, fFR = 80Hz, case of 1/480 duty operation, No-load

AC CHARACTERISTICS

Timing Characteristics of SEG Mode



SEG Mode 1

(VSS = V5 = 0V, V_{DD} = 4.5 - 5.5V, V0 = 15 to 42, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWCK	71	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	tWCKH	23	-		ns	
Shift clock "L" pulse width	tWCKL	23	-		ns	
Data setup time	tDS	10	-		ns	
Data hold time	tDH	20	-		ns	
Latch pulse "H" pulse width	tWLPH	23	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	25	-		ns	
Latch pulse rise to Shift clock rise time	tLS	25	-		ns	
Latch pulse fall to Shift clock rise time	tLH	25	-		ns	
Input signal rise time	tr		-	50	ns	Note 2
Input signal fall time	tf		-	50	ns	Note 2
Enable setup time	tS	21	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-		μs	
Output delay time (1)	tD		-	40	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2		-	1.2	μs	CL = 15pF
Output delay time (3)	tpd3		-	1.2	μs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (Tck - tWCKII - twckI)/2 is the maximum in the case of high speed operation.

SEG Mode 2

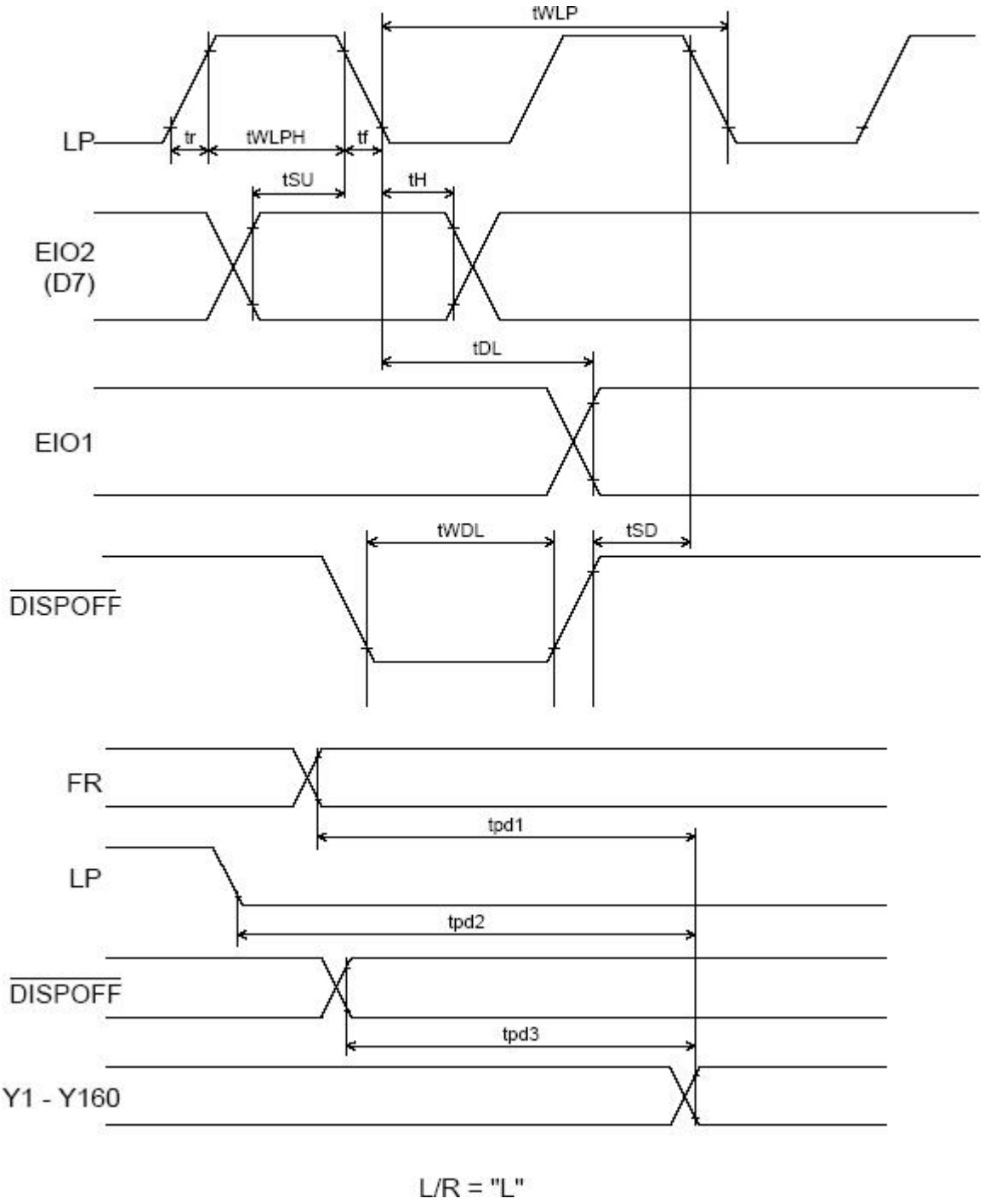
(VSS = V5 = 0V, V_{DD} = 2.5 - 4.5V, V0 = 15 to 42, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWCK	125	-		ns	tr, tf ≦ 11ns, Note 1
Shift clock "H" pulse width	tWCKH	51	-		ns	
Shift clock "L" pulse width	tWCKL	51	-		ns	
Data setup time	tDS	30	-		ns	
Data hole time	tDH	40	-		ns	
Latch pulse "H" pulse width	tWLPH	51	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	51	-		ns	
Latch pulse rise to Shift clock rise time	tLS	51	-		ns	
Latch pulse fall to Shift clock fall time	tLH	51	-		ns	
Input signal rise time	tr		-	50	ns	Note 2
Input signal fall time	tf		-	50	ns	Note 2
Enable setup time	tS	36	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-		μs	
Output delay time (1)	tD		-	78	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2		-	1.2	μs	CL = 15pF
Output delay time (3)	tpd3		-	1.2	μs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (tCK - tWCKII - tWCKL)/2 is the maximum in the case of high speed operation.

Timing Characteristics of COM Mode



L/R = "L"

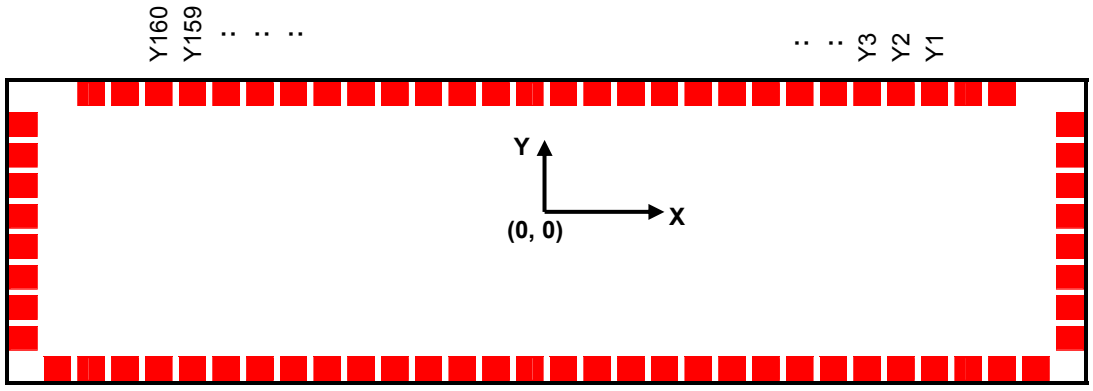
COM Mode

(VSS = V5 = 0V, V_{DD} = 2.5 - 5.5V, V0 = 15 to 42V and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWLP	250	-	-	ns	tr, tf ≦ 20ns
Shift clock "H" pulse width	tWLPH	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	tSU	30	-	-	ns	
Data hole time	tH	50	-	-	ns	
Input signal rise time	tr		-	50	ns	
Input signal fall time	tf		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-	-	μs	
Output delay time (1)	tDL	-	-	200	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2	-	-	1.2	μs	CL = 15pF
Output delay time (3)	tpd3	-	-	1.2	μs	CL = 15pF

PHYSICAL DIMENSIONS

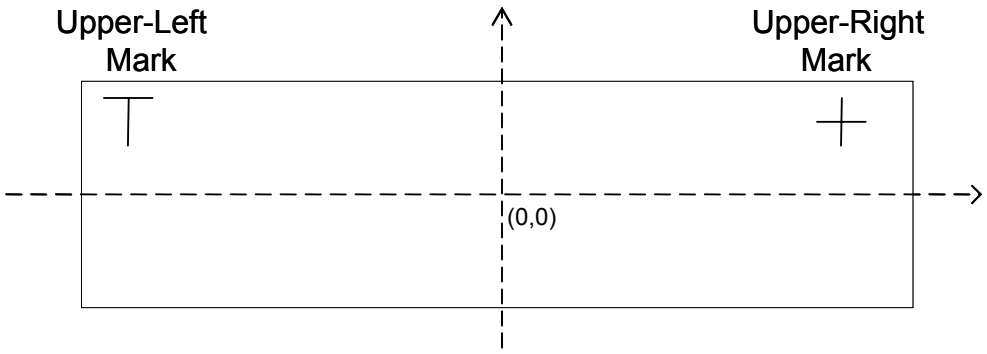
Circuit / Bump View:



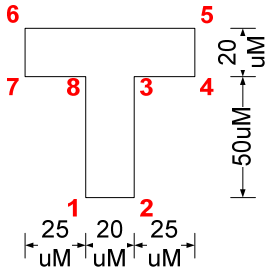
Die / Bump Information:

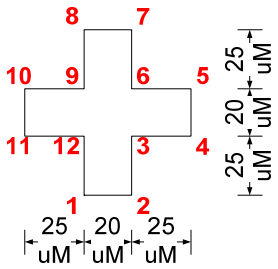
Die Size:	7396 µM x 933 µM ± 40 µM	Bump Size (Typical):	31 µM x 68 µM ± 2 µM
Die Thickness:	508 µM ± 20 µM	Bump Pitch:	43 µM
Bump Height:	15 µM ± 3 µM	Bump Gap:	12 µM
	(H_{MAX} – H_{MIN}) within die ⩽ 2 µM	Coordinate origin:	Chip center
		Pad reference:	Pad center

ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:

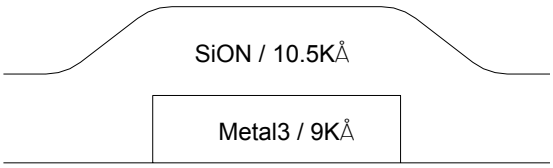




COORDINATES:

Point	U-Left Mark (T)		U-Right Mark (+)	
	X	Y	X	Y
1	-3623	346.3	3603	346.3
2	-3603	346.3	3623	346.3
3	-3603	396.3	3623	371.3
4	-3578	396.3	3648	371.3
5	-3578	416.3	3648	391.3
6	-3648	416.3	3623	391.3
7	-3648	396.3	3623	416.3
8	-3623	396.3	3603	416.3
9	–	–	3603	391.3
10	–	–	3578	391.3
11	–	–	3578	371.3
12	–	–	3603	371.3

TOP METAL AND PASSIVATIO



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

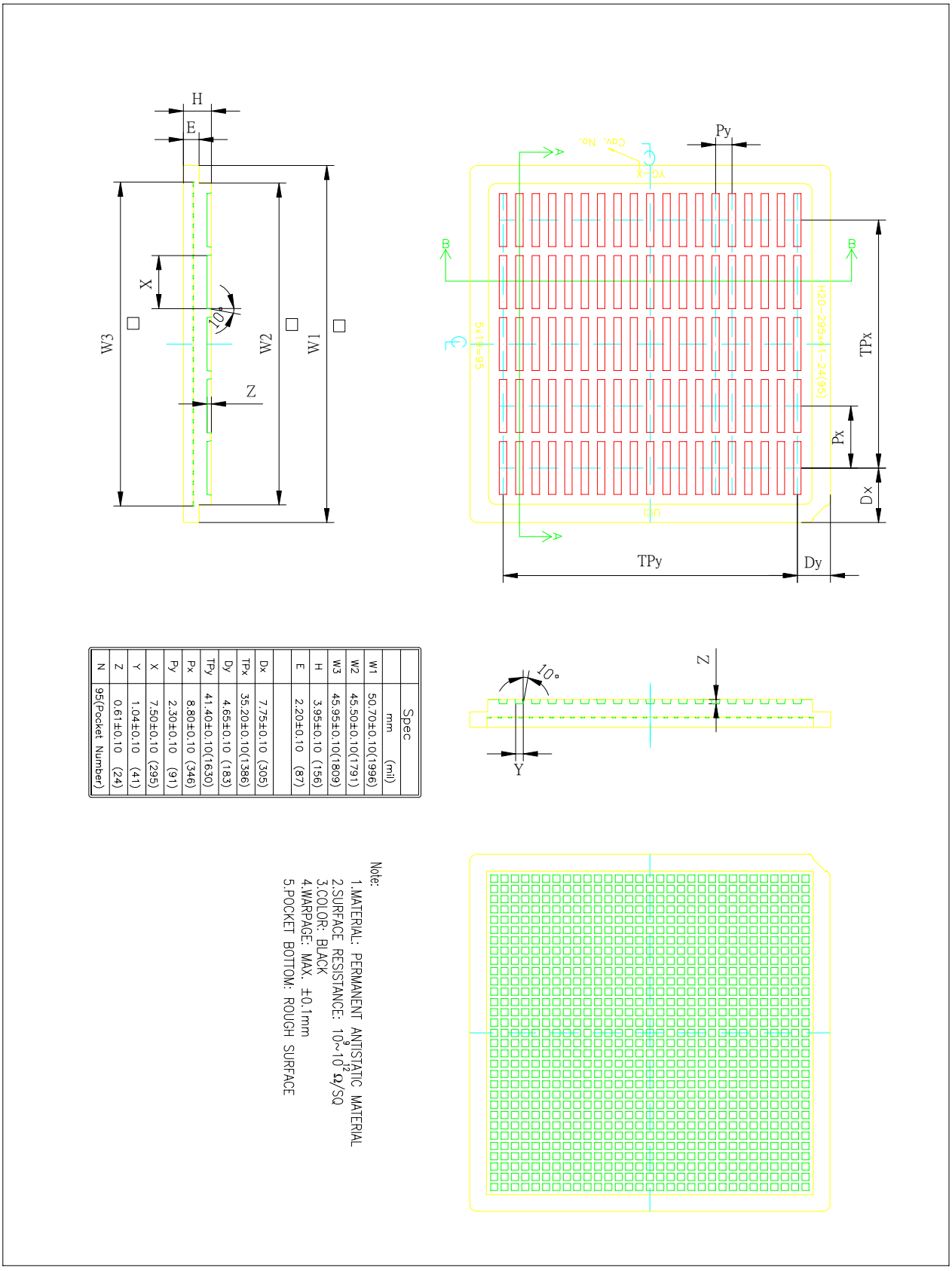
#	Name	X	Y	W	H
1	DUMMY	-3597.2	-384.3	77.6	40
2	V5	-3438.6	-384.3	77.6	40
3	DUMMY	-3315.5	-384.3	77.6	40
4	VSS	-3192.4	-384.3	77.6	40
5	DUMMY	-3069.3	-384.3	77.6	40
6	VSS	-2946.2	-384.3	77.6	40
7	DUMMY	-2823.1	-384.3	77.6	40
8	VSS	-2600	-384.3	77.6	40
9	VSS	-2400	-384.3	77.6	40
10	L/R	-2200	-384.3	77.6	40
11	VDD	-2000	-384.3	77.6	40
12	VDD	-1800	-384.3	77.6	40
13	S/C	-1600	-384.3	77.6	40
14	VSS	-1400	-384.3	77.6	40
15	EIO2	-1200	-384.3	77.6	40
16	DI0	-1000	-384.3	77.6	40
17	DI1	-800	-384.3	77.6	40
18	DI2	-600	-384.3	77.6	40
19	DI3	-400	-384.3	77.6	40
20	DI4	-200	-384.3	77.6	40
21	DI5	0	-384.3	77.6	40
22	DI6	200	-384.3	77.6	40
23	DI7	400	-384.3	77.6	40
24	VSS	600	-384.3	77.6	40
25	XCK	800	-384.3	77.6	40
26	VSS	1000	-384.3	77.6	40
27	/DISPOFF	1200	-384.3	77.6	40
28	LP	1400	-384.3	77.6	40
29	EIO1	1600	-384.3	77.6	40
30	FR	1800	-384.3	77.6	40
31	VDD	2000	-384.3	77.6	40
32	MD	2200	-384.3	77.6	40
33	VSS	2400	-384.3	77.6	40
34	VSS	2600	-384.3	77.6	40
35	DUMMY	2823.1	-384.3	77.6	40
36	VSS	2946.2	-384.3	77.6	40
37	DUMMY	3069.3	-384.3	77.6	40
38	VSS	3192.4	-384.3	77.6	40
39	DUMMY	3315.5	-384.3	77.6	40
40	V5	3438.6	-384.3	77.6	40
41	DUMMY	3597.2	-384.3	77.6	40
42	V34	3616	-288	40	77.6
43	DUMMY	3616	-164.9	40	77.6
44	V12	3616	-41.8	40	77.6
45	DUMMY	3616	81.3	40	77.6
46	V0	3616	204.4	40	77.6
47	DUMMY	3547.5	387.3	31	68
48	DUMMY	3504.5	387.3	31	68
49	Y1	3461.5	387.3	31	68
50	Y2	3418.5	387.3	31	68
51	Y3	3375.5	387.3	31	68
52	Y4	3332.5	387.3	31	68
53	Y5	3289.5	387.3	31	68
54	Y6	3246.5	387.3	31	68
55	Y7	3203.5	387.3	31	68
56	Y8	3160.5	387.3	31	68
57	Y9	3117.5	387.3	31	68

#	Name	X	Y	W	H
58	Y10	3074.5	387.3	31	68
59	Y11	3031.5	387.3	31	68
60	Y12	2988.5	387.3	31	68
61	Y13	2945.5	387.3	31	68
62	Y14	2902.5	387.3	31	68
63	Y15	2859.5	387.3	31	68
64	Y16	2816.5	387.3	31	68
65	Y17	2773.5	387.3	31	68
66	Y18	2730.5	387.3	31	68
67	Y19	2687.5	387.3	31	68
68	Y20	2644.5	387.3	31	68
69	Y21	2601.5	387.3	31	68
70	Y22	2558.5	387.3	31	68
71	Y23	2515.5	387.3	31	68
72	Y24	2472.5	387.3	31	68
73	Y25	2429.5	387.3	31	68
74	Y26	2386.5	387.3	31	68
75	Y27	2343.5	387.3	31	68
76	Y28	2300.5	387.3	31	68
77	Y29	2257.5	387.3	31	68
78	Y30	2214.5	387.3	31	68
79	Y31	2171.5	387.3	31	68
80	Y32	2128.5	387.3	31	68
81	Y33	2085.5	387.3	31	68
82	Y34	2042.5	387.3	31	68
83	Y35	1999.5	387.3	31	68
84	Y36	1956.5	387.3	31	68
85	Y37	1913.5	387.3	31	68
86	Y38	1870.5	387.3	31	68
87	Y39	1827.5	387.3	31	68
88	Y40	1784.5	387.3	31	68
89	Y41	1741.5	387.3	31	68
90	Y42	1698.5	387.3	31	68
91	Y43	1655.5	387.3	31	68
92	Y44	1612.5	387.3	31	68
93	Y45	1569.5	387.3	31	68
94	Y46	1526.5	387.3	31	68
95	Y47	1483.5	387.3	31	68
96	Y48	1440.5	387.3	31	68
97	Y49	1397.5	387.3	31	68
98	Y50	1354.5	387.3	31	68
99	Y51	1311.5	387.3	31	68
100	Y52	1268.5	387.3	31	68
101	Y53	1225.5	387.3	31	68
102	Y54	1182.5	387.3	31	68
103	Y55	1139.5	387.3	31	68
104	Y56	1096.5	387.3	31	68
105	Y57	1053.5	387.3	31	68
106	Y58	1010.5	387.3	31	68
107	Y59	967.5	387.3	31	68
108	Y60	924.5	387.3	31	68
109	Y61	881.5	387.3	31	68
110	Y62	838.5	387.3	31	68
111	Y63	795.5	387.3	31	68
112	Y64	752.5	387.3	31	68
113	Y65	709.5	387.3	31	68
114	Y66	666.5	387.3	31	68

#	Name	X	Y	W	H
115	Y67	623.5	387.3	31	68
116	Y68	580.5	387.3	31	68
117	Y69	537.5	387.3	31	68
118	Y70	494.5	387.3	31	68
119	Y71	451.5	387.3	31	68
120	Y72	408.5	387.3	31	68
121	Y73	365.5	387.3	31	68
122	Y74	322.5	387.3	31	68
123	Y75	279.5	387.3	31	68
124	Y76	236.5	387.3	31	68
125	Y77	193.5	387.3	31	68
126	Y78	150.5	387.3	31	68
127	Y79	107.5	387.3	31	68
128	Y80	64.5	387.3	31	68
129	DUMMY	21.5	387.3	31	68
130	DUMMY	-21.5	387.3	31	68
131	Y81	-64.5	387.3	31	68
132	Y82	-107.5	387.3	31	68
133	Y83	-150.5	387.3	31	68
134	Y84	-193.5	387.3	31	68
135	Y85	-236.5	387.3	31	68
136	Y86	-279.5	387.3	31	68
137	Y87	-322.5	387.3	31	68
138	Y88	-365.5	387.3	31	68
139	Y89	-408.5	387.3	31	68
140	Y90	-451.5	387.3	31	68
141	Y91	-494.5	387.3	31	68
142	Y92	-537.5	387.3	31	68
143	Y93	-580.5	387.3	31	68
144	Y94	-623.5	387.3	31	68
145	Y95	-666.5	387.3	31	68
146	Y96	-709.5	387.3	31	68
147	Y97	-752.5	387.3	31	68
148	Y98	-795.5	387.3	31	68
149	Y99	-838.5	387.3	31	68
150	Y100	-881.5	387.3	31	68
151	Y101	-924.5	387.3	31	68
152	Y102	-967.5	387.3	31	68
153	Y103	-1010.5	387.3	31	68
154	Y104	-1053.5	387.3	31	68
155	Y105	-1096.5	387.3	31	68
156	Y106	-1139.5	387.3	31	68
157	Y107	-1182.5	387.3	31	68
158	Y108	-1225.5	387.3	31	68
159	Y109	-1268.5	387.3	31	68
160	Y110	-1311.5	387.3	31	68
161	Y111	-1354.5	387.3	31	68
162	Y112	-1397.5	387.3	31	68
163	Y113	-1440.5	387.3	31	68
164	Y114	-1483.5	387.3	31	68
165	Y115	-1526.5	387.3	31	68
166	Y116	-1569.5	387.3	31	68

#	Name	X	Y	W	H
167	Y117	-1612.5	387.3	31	68
168	Y118	-1655.5	387.3	31	68
169	Y119	-1698.5	387.3	31	68
170	Y120	-1741.5	387.3	31	68
171	Y121	-1784.5	387.3	31	68
172	Y122	-1827.5	387.3	31	68
173	Y123	-1870.5	387.3	31	68
174	Y124	-1913.5	387.3	31	68
175	Y125	-1956.5	387.3	31	68
176	Y126	-1999.5	387.3	31	68
177	Y127	-2042.5	387.3	31	68
178	Y128	-2085.5	387.3	31	68
179	Y129	-2128.5	387.3	31	68
180	Y130	-2171.5	387.3	31	68
181	Y131	-2214.5	387.3	31	68
182	Y132	-2257.5	387.3	31	68
183	Y133	-2300.5	387.3	31	68
184	Y134	-2343.5	387.3	31	68
185	Y135	-2386.5	387.3	31	68
186	Y136	-2429.5	387.3	31	68
187	Y137	-2472.5	387.3	31	68
188	Y138	-2515.5	387.3	31	68
189	Y139	-2558.5	387.3	31	68
190	Y140	-2601.5	387.3	31	68
191	Y141	-2644.5	387.3	31	68
192	Y142	-2687.5	387.3	31	68
193	Y143	-2730.5	387.3	31	68
194	Y144	-2773.5	387.3	31	68
195	Y145	-2816.5	387.3	31	68
196	Y146	-2859.5	387.3	31	68
197	Y147	-2902.5	387.3	31	68
198	Y148	-2945.5	387.3	31	68
199	Y149	-2988.5	387.3	31	68
200	Y150	-3031.5	387.3	31	68
201	Y151	-3074.5	387.3	31	68
202	Y152	-3117.5	387.3	31	68
203	Y153	-3160.5	387.3	31	68
204	Y154	-3203.5	387.3	31	68
205	Y155	-3246.5	387.3	31	68
206	Y156	-3289.5	387.3	31	68
207	Y157	-3332.5	387.3	31	68
208	Y158	-3375.5	387.3	31	68
209	Y159	-3418.5	387.3	31	68
210	Y160	-3461.5	387.3	31	68
211	DUMMY	-3504.5	387.3	31	68
212	DUMMY	-3547.5	387.3	31	68
213	V0	-3616	204.4	40	77.6
214	DUMMY	-3616	81.3	40	77.6
215	V12	-3616	-41.8	40	77.6
216	DUMMY	-3616	-164.9	40	77.6
217	V34	-3616	-288	40	77.6

TRAY INFORMATION



	Spec	
	mm	(mil)
W1	50.70±0.10	(1996)
W2	45.50±0.10	(1791)
W3	45.95±0.10	(1809)
H	3.95±0.10	(156)
E	2.20±0.10	(87)
Dx	7.75±0.10	(305)
TPx	35.20±0.10	(1386)
Dy	4.65±0.10	(183)
TPy	41.40±0.10	(1630)
Px	8.80±0.10	(346)
Py	2.30±0.10	(91)
X	7.50±0.10	(295)
Y	1.04±0.10	(41)
Z	0.61±0.10	(24)
N	95(Pocket Number)	

Note:
1.MATERIAL: PERMANENT ANTISTATIC MATERIAL
2.SURFACE RESISTANCE: 10^9~10^{12} Ω/SQ
3.COLOR: BLACK
4.WARPAGE: MAX. ±0.1mm
5.POCKET BOTTOM: ROUGH SURFACE

REVISION HISTORY

Revision	Contents	Date
0.6	First Release	Oct. 14, 2011
1.0	(1) Part Number is corrected. (2) Tray drawing presents.	Mar. 13, 2012
1.1	(1) Part Number for “Bump on Chip Tray” is modified. (2) Die Size is corrected.	Apr. 2, 2012