# OLED DISPLAY SPECIFICATION


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# RET025664A

## General Specification

The Features is described as follow:

- Module Dimension: 84.0 × 25.8 × 2.15 mm
- Active Area: 69.098 × 17.258 mm
- Dot Matrix: 256 * 64
- Pixel Size: 0.248 × 0.248 mm
- Pixel Pitch: 0.27 × 0.27 mm
- Duty: 1/64 Duty
- Display Mode: Passive Matrix
- Display Color: Monochrome
- IC: SSD1322 COF
- Interface: 6800, 8080, SPI
- Size: 2.8-inch

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# Interface Pin Function

| Pin Number | Symbol | I/O | Function |
|---|---|---|---|
| ***Power Supply*** | | | |
| **26** | **VCI** | P | ***Power Supply for Operation***<br>This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO. |
| **25** | **VDD** | P | ***Power Supply for Core Logic Circuit***<br>This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances. |
| **24** | **VDDIO** | P | ***Power Supply for I/O Pin***<br>This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO. |
| **2** | **VSS** | P | ***Ground of Logic Circuit***<br>This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground. |
| **3,29** | **VCC** | P | ***Power Supply for OLED Panel***<br>These are the most positive voltage supply pin of the chip. They must be connected to external source. |
| **5,28** | **VLSS** | P | ***Ground of Analog Circuit***<br>These are the analog ground pins. They should be connected to VSS externally. |
| ***Driver*** | | | |
| **22** | **IREF** | I | ***Current Reference for Brightness Adjustment***<br>This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than |

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<table>
<tr><td></td><td></td><td></td><td>10uA.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>P</td><td>Voltage Output High Level for COM Signal<br>This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>27</td><td>VSL</td><td>P</td><td>Voltage Output Low Level for SEG Signal<br>This is segment voltage reference pin.<br>When external VSL is not used, this pin should be left open.<br>When external VSL is used, this pin should connect with resistor and diode to ground.</td></tr>
<tr><td colspan="4">Testing Pads</td></tr>
<tr><td>21</td><td>FR</td><td>O</td><td>Frame Frequency Triggering Signal<br>This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.</td></tr>
<tr><td>16</td><td>BS0</td><td rowspan="2">I</td><td rowspan="2">Communicating Protocol Select<br>These pins are MCU interface selection input. See the following table:<br><table><tr><td></td><td>BS0</td><td>BS1</td></tr><tr><td>3-wire SPI</td><td>1</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr></table></td></tr>
<tr><td>17</td><td>BS1</td></tr>
<tr><td>20</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver<br>This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select<br>This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>18</td><td>D/C#</td><td>I</td><td>Data/Command Control<br>This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data.<br>When the pin is pulled low, the input at D7~D0 will be transferred</td></tr>
</table>

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| | | | |
|---|---|---|---|
| | | | to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. |
| **14** | **E/RD#** | I | ***Read/Write Enable or Read***<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.<br>When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.<br>When serial mode is selected, this pin must be connected to VSS. |
| **15** | **R/W#** | I | ***Read/Write Select or Write***<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.<br>When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.<br>When serial mode is selected, this pin must be connected to VSS. |
| **6~13** | **D7~D0** | I/O | ***Host Data Input/Output Bus***<br>These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.<br>Unused pins must be connected to VSS except for D2 in serial mode |
| ***Reserve*** | | | |
| **23** | **N.C.** | - | ***Reserved Pin***<br>The N.C. pin between function pins are reserved for compatible and flexible design. |

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| | | | |
|---|---|---|---|
| **1,30** | **N.C. (GND)** | - | ***Reserved Pin*** (Supporting Pin)<br>The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground. |

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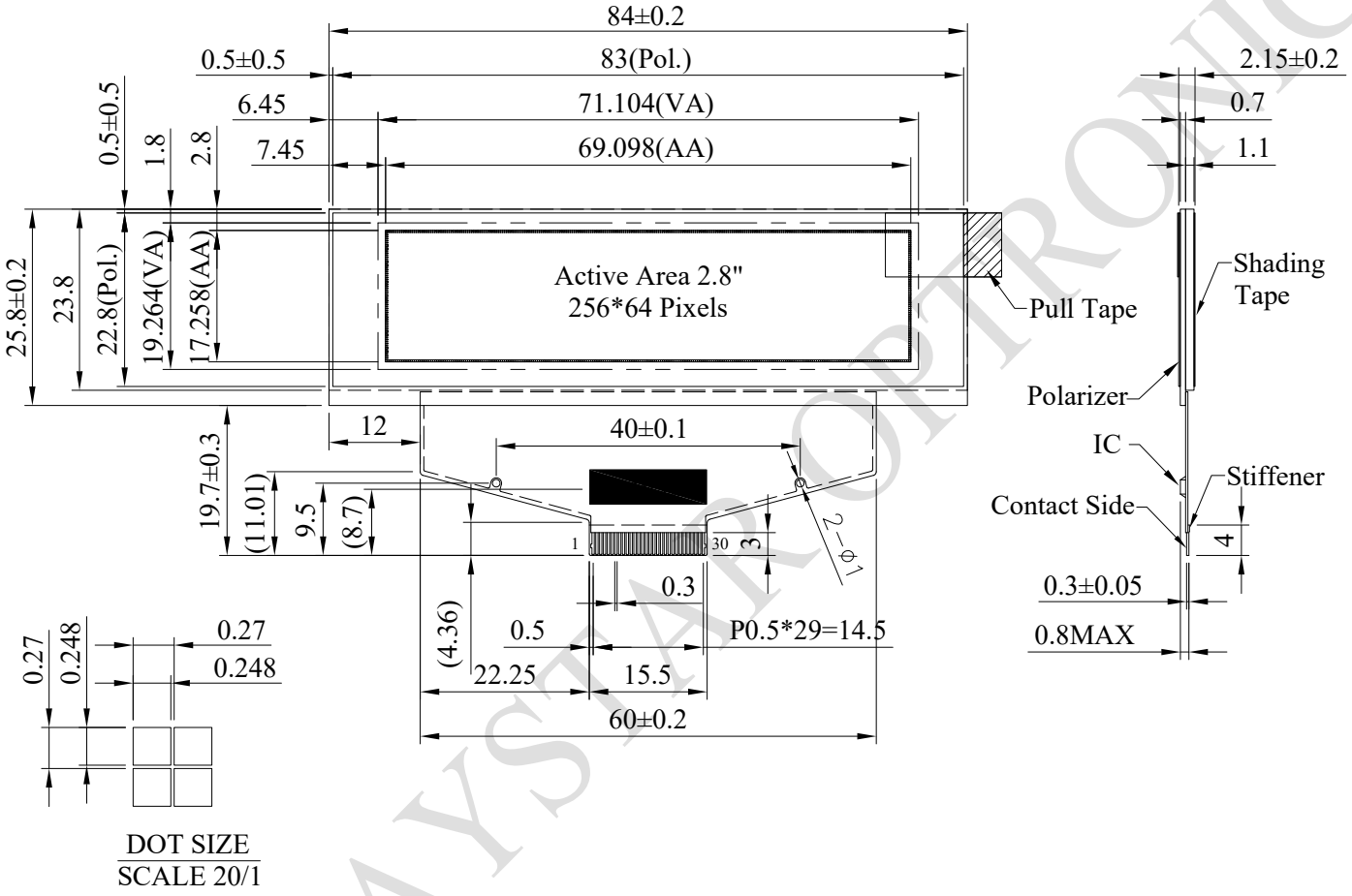
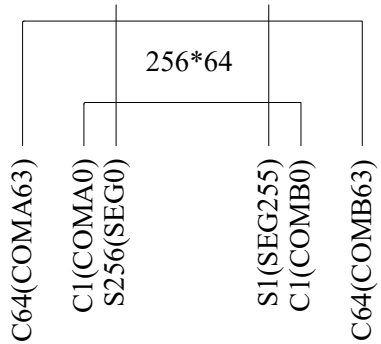
# Counter Drawing




| PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|
| 1 | NC(GND) | 16 | BS0 |
| 2 | VSS | 17 | BS1 |
| 3 | VCC | 18 | DC# |
| 4 | VCOMH | 19 | CS# |
| 5 | VLSS | 20 | RES# |
| 6 | D7 | 21 | FR |
| 7 | D6 | 22 | IREF |
| 8 | D5 | 23 | NC |
| 9 | D4 | 24 | VDDIO |
| 10 | D3 | 25 | VDD |
| 11 | D2 | 26 | VCI |
| 12 | D1 | 27 | VSL |
| 13 | D0 | 28 | VLSS |
| 14 | E/RD# | 29 | VCC |
| 15 | R/W# | 30 | NC(GND) |




The non-specified tolerance of dimension is ±0.3mm.

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# Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage for Logic | VDD | -0.5 | 2.75 | V |
| Low Voltage Power Supply | VCI | -0.3 | 4.0 | V |
| Power Supply for I/O Pins | VDDIO | -0.5 | VCI | V |
| Supply Voltage for Display | VCC | -0.5 | 20.0 | V |
| Operating Temperature | TOP | -40 | +80 | °C |
| Storage Temperature | TSTG | -40 | +85 | °C |

# Electrical Characteristics

## DC Electrical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage for Logic | VCI | Note | 2.8 | 3.0 | 3.3 | V |
| Supply Voltage for Display | VCC | — | 14 | 14.5 | 15 | V |
| High Level Input | VIH | — | 0.8×VDDIO | — | VDDIO | V |
| Low Level Input | VIL | — | 0 | — | 0.2×VDDIO | V |
| High Level Output | VOH | — | 0.9×VDDIO | — | VDDIO | V |
| Low Level Output | VOL | — | 0 | — | 0.1×VDDIO | V |
| 50% Check Board Operating Current | | VCC =14.5V | — | 30 | 32 | mA |

Note: Supply Voltage for Logic = VDD core power supply can be regulated from VCI.

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