OLED DISPLAY SPECIFICATION

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REP012864U-CTP

General Specification

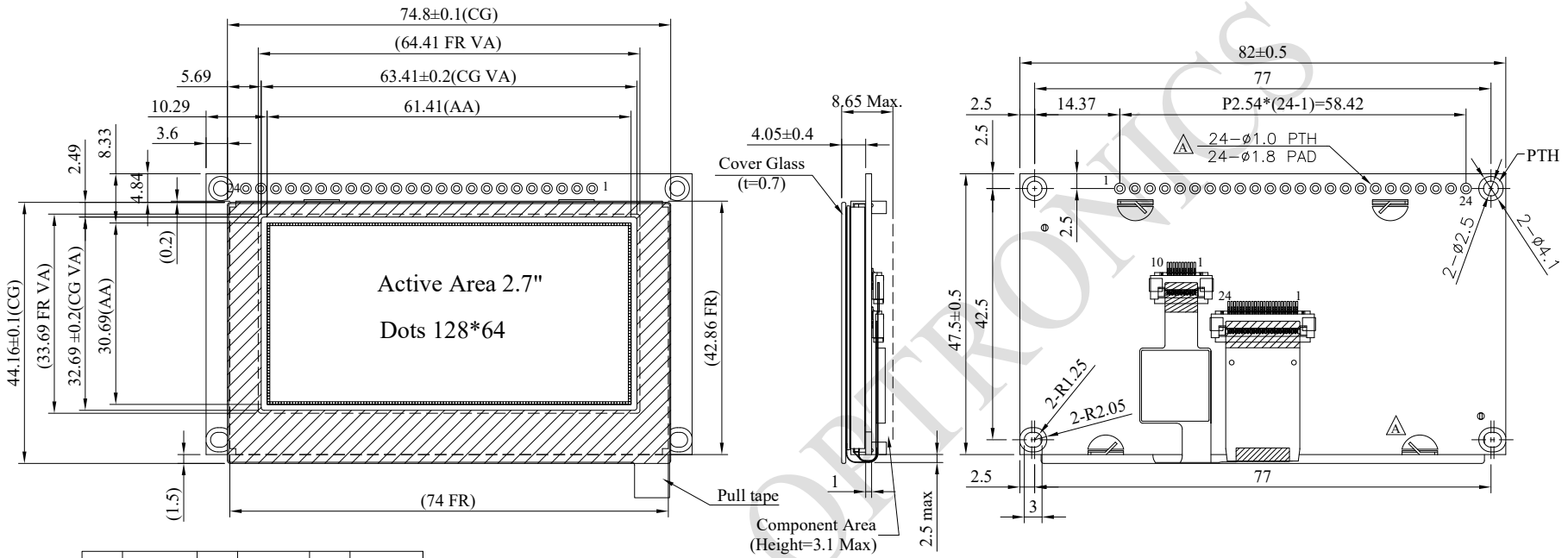
- Module dimension: 82.0 × 47.5 × 8.65 Max.mm
- Active area: 61.41 x 30.69 mm
- Dot Matrix: 128 x 64 Dots
- Pixel Size:0.45 x 0.45 mm
- Pixel Pitch: 0.48 x 0.48 mm
- Display Mode: Passive Matrix
- Duty: 1/64 Duty
- Gray Scale: 4 bits
- Display Color: Monochrome
- OLED IC: SSD1357
- OLED Interface: 8-bits 6800 and 8080 parallel, 4-line SPI, I2C
- Size: 2.7 inch
- CTP IC: GT911
- Detect Point:1
- CTP Interface: I2C
- Surface: Normal Glare

Interface Pin Function

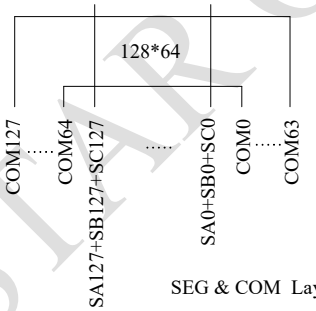
No.	Symbol	Function
1	VSS	This is a ground pin.
2	VDD	Power supply pin for core logic operation
3	NC	Reserved Pin The N.C. pin between function pins is reserved for compatible and flexible design.
4	D/C#	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I2C mode, this pin acts as SA0 for slave address selection.
5	R/W# (WR#)	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
6	E/RD#	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
7	DB0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	NC	No connection

<table>
<tr><td>16</td><td>RES#</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>17</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>18</td><td>NC</td><td>No connection</td></tr>
<tr><td>19</td><td>BS2</td><td rowspan="2">Communicating Protocol Select.
These pins are MCU interface selection input. See the following table:<table><tr><td></td><td>BS1</td><td>BS2</td></tr><tr><td>I2C</td><td>1</td><td>0</td></tr><tr><td>4-wire Serial</td><td>0</td><td>0</td></tr><tr><td>8-bit 8080 Parallel</td><td>1</td><td>1</td></tr><tr><td>8-bit 6800 Parallel</td><td>0</td><td>1</td></tr></table></td></tr>
<tr><td>20</td><td>BS1</td></tr>
<tr><td>21</td><td>TP_SCK</td><td>I2C clock signal</td></tr>
<tr><td>22</td><td>TP_SDA</td><td>I2C data signal</td></tr>
<tr><td>23</td><td>TP_INT</td><td>Interrupt signal, active low, asserted to request
Host start a new transaction</td></tr>
<tr><td>24</td><td>TP_RST</td><td>External reset signal, active low</td></tr>
</table>

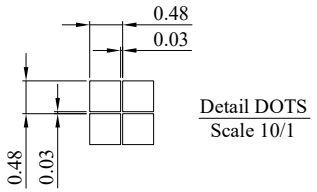
Contour Drawing



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	9	DB2	17	CS#
2	VDD	10	DB3	18	NC
3	NC	11	DB4	19	BS2
4	D/C#	12	DB5	20	BS1
5	R/W#(WR#)	13	DB6	21	TP_SCK
6	E(/RD#)	14	DB7	22	TP_SDA
7	DB0	15	NC	23	TP_INT
8	DB1	16	RES#	24	TP_RST



SEG & COM Layout



Detail DOTS
Scale 10/1

The non-specified tolerance of dimension is ±0.3 mm .

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage for Logic	VDD	-0.3	4.0	V
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TSTG	-30	+80	°C

Electrical Characteristics

DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	—	2.8	3.0	3.3	V
High Level Input	VIH	—	0.8×VDD	—	—	V
Low Level Input	VIL	—	—	—	0.2×VDD	V
High Level Output	VOH	—	0.9×VDD	—	—	V
Low Level Output	VOL	—	—	—	0.1×VDD	V
50% Check Board operating Current	IDD	VDD =3V	—	160	240	mA